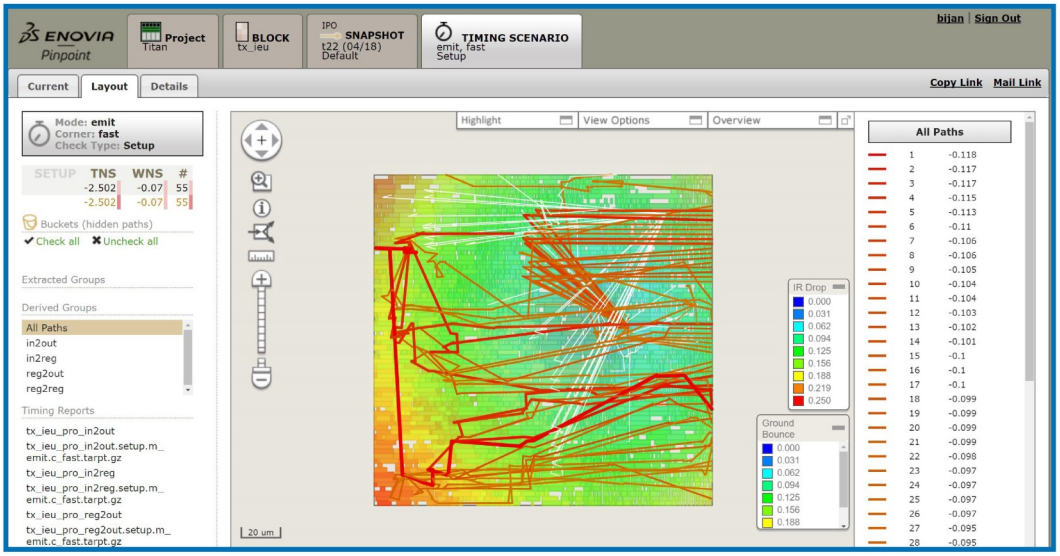
Consensia

DASSAULT SYSTEMES

Pinpoint Analytics for ASIC/SOC & FPGA Design Closure

Pinpoint is an advanced, web-based analytics platform that provides comprehensive analysis of digital design flows for ASIC/SOC and FPGA design teams. It helps designers to quickly identify potential issues and bottlenecks by assimilating real time data from every aspect of the design flow from synthesis to layout.



View Metrics from Multiple Sources - Pinpoint's 'connectivity aware' capability enables timing paths and power to be viewed over layout

Pinpoint helps reduce risk by providing ASIC and FPGA design teams with a scalable, customizable analytics solution for monitoring design progress.

Product Overview

Pinpoint helps reduce risk and lower overall project costs by providing ASIC, SOC and FPGA design teams with real time progress and status information about each phase of the design cycle. Pinpoint assimilates data from multiple sources – synthesis, STA, power, layout, physical verification, etc. – and intelligently displays this data in customizable dashboards that provide a holistic view of the progress of each phase of the design and maturity of the overall design.

Key Features

Web based Analysis for Collaborative Design

- Pinpoint extracts design information from tool reports, log files and LEF/DEF so it's non-disruptive to your design flow
- Reports and metrics are displayed as web based, real time updates, so designers can spend more time debugging instead of preparing for design reviews
- Share links to dynamic reports or layout views across geographically dispersed design centers and collaborate in real time on web meetings to resolve design issues quickly

Powerful Integrated Analytics Capability

- Designers can view full chip and block level metrics, for individual functions, i.e.STA, or view metrics from multiple sources in one report- e.g. view inter-or intra-block timing paths with hierarchy over a layout view (in Pinpoint)

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'Out of the Box' Ease of Use

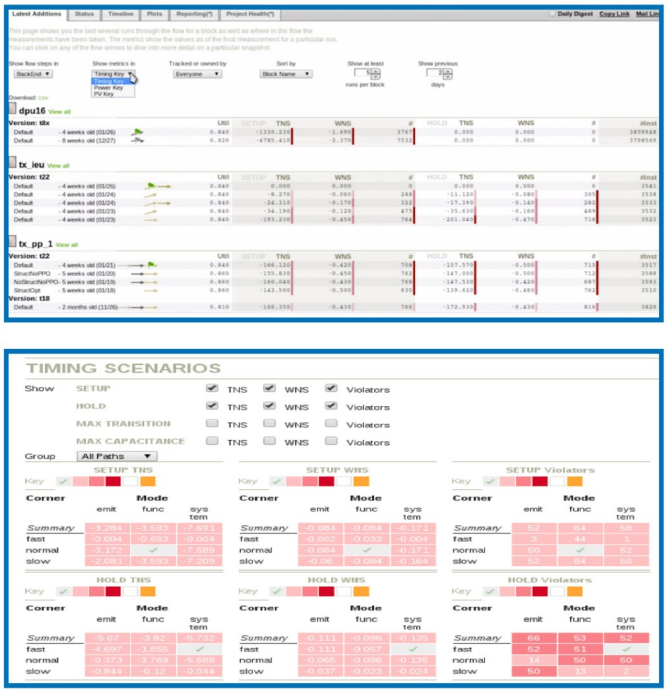
- Pinpoint is tool agnostic, so it can import data from any EDA vendor tool flow or point tool
- Out of the box support for common EDA tools with many pre-configured reports enables immediate reporting on design flow progress

Connectivity Aware Layout for Detailed Reporting

- Pinpoint's connectivity aware processing engine understands every instance in your design, including hierarchy, so it can provide interactive metrics about your design – including DRC violations, location of timing path violations, etc.

API for Integrating Custom Reporting

- Flexible API enables rapid integration of existing in-house developed metrics or 3rd party produced metrics with Pinpoint
- New custom reports can easily be created from existing data, or as new tools are added to your design flow



View timing progress with Total Negative Slack, Worst Negative Slack in tabular form, then click on a specific run to view timing corners, and violators for SetUp, Hold, Max. Capacitance, etc. in color coded Timing Corner/-Mode diagrams

Benefits

- No more struggling with designs being 95% complete for 30% of design cycle time - Pinpoint's comprehensive trend analysis and illustration of all issues in one dashboard lets you can visualize how close you are to design closure
- Pinpoint's out-of-the-box timing reports provide a detailed and filterable list of timing paths that facilitate a structured approach to STA diagnostics
- Pinpoint's reporting format enables designers to run design experimentations by uniquifying each runs so you can identify an optimal set of constraints as a starting point
- View layout reporting and metrics in Pinpoint, so no need to 'check out' expensive APR tools

ASIC/SOC Designers

Pinpoint enables designers to increase productivity and Turn Around Time by identifying and collaboratively addressing issues at every flow step – from STA, IR or EM analysis to layout and physical verification

Designers can also see the impact of STA, power analysis, etc., on the physical layout using Pinpoint's unique capability to overlay IR heat map, timing paths and DRCs over a layout view

Web based dashboards provide real time information to the entire design team, eliminating preparation time for design reviews

Design Managers

Design managers can anticipate and address potential bottle-necks that may delay tape out by using a summary dashboard containing the overall design metrics for every flow step This enables design managers to move resources to the appropriate areas of the design to help eliminate delays

Layout Engineers

Layout engineers are able to quickly identify layout problems, including P&R resources, or locating and categorizing DRCs to reduce DRC count faster

Engineering Management

Pinpoint's custom dashboard capability delivers all the critical metrics on one dashboard so that management can under-stand real time progress of each design and see a day to day trend line to indicate realistic time to design closure

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